(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 891 045 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.01.1999 Bulletin 1999/02

(51) Int. Cl.[6]: H03K 19/003

(21) Application number: 98104191.6

(22) Date of filing: 09.03.1998

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 11.07.1997 US 893434

(71) Applicant:
Hewlett-Packard Company
Palo Alto, California 94304 (US)

(72) Inventors:
- Naffziger, Samuel D.
Fort Collins, CO 80525 (US)
- Yetter, Jeffry D.
Loveland, CO 80538 (US)

(74) Representative:
Schoppe, Fritz, Dipl.-Ing.
Schoppe & Zimmermann
Patentanwälte
Postfach 71 08 67
81458 München (DE)

(54) A coupling charge compensation device for VLSI circuits

(57) A circuit for reducing capacitive coupling between a culprit (202) and a victim (212) signal line is provided which comprises two inverters, a n-channel FET (222) connected as a capacitor, and a p-channel FET (220) connected as a capacitor. The input of both inverters are connected to the culprit line (202). The first inverter (204, 206) is designed to respond to high-to-low transition on the culprit line more rapidly than a low-to-high transition. The output of the first inverter (230) is connected to the drain and source of the n-channel FET (222). The gate of the n-channel FET (222) is connected to the victim line (212). The second inverter (208, 210) is designed to respond to low-to-high transition on the culprit line (202) more rapidly than a high-to-low transition. The output of the second inverter (232) is connected to the drain and source of the p-channel FET (220). The gate of the p-channel FET is connected to the victim line (212).

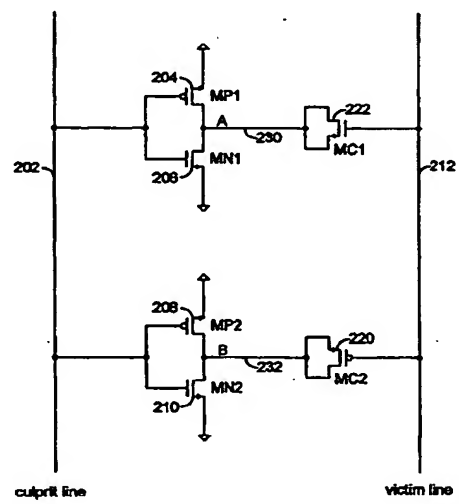


FIG. 2

Printed by Xerox (UK) Business Services
2.16.7/3.6

BNSDOCID: <EP_______0891045A1_I_>

Description

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to electronic circuits. In particular this invention relates to integrated electronic circuits for reducing the effects of charge coupling between wires on a VLSI chip.

Background of the Invention

On a VLSI integrated circuit, such as a microprocessor, some signal lines may be routed adjacent to each other over relatively large distances. This may be necessary because the signals have a common source and destination; are part of a large multi-bit bus, or were coincidentally routed adjacent to each other by a automated router. Unfortunately, this arrangement causes problems that may lead to unreliable, or incorrect, functioning of the integrated circuit.

When at least one of the signal lines switches (the culprit) while at least one of the other signals is attempting to remain at its previous value (the victim), the capacitance between the switching line (or lines) will cause the victim line to "glitch" as charge is capacitively transferred between the culprit line(s) and the victim line. This "glitch" can cause failures when, for example, it causes the victim line to rise above a gate threshold voltage from ground, turning on an n-channel FET (field effect transistor) whose gate is connected to the victim line.

One solution to this problem is to increase the spacing between signal lines. This reduces the amount of charge coupled from the culprit(s) to the victim by decreasing the capacitance between them. However, this is undesirable because it increases the cost of the integrated circuit by reducing the overall density of the VLSI integrated circuit.

Another solution is to add a "ballast" capacitor connected between the victim signal and a power supply. This reduces the amount of "glitch" voltage change that occurs by increasing the overall capacitance of the victim line. However, this is undesirable because the "ballast" capacitor burdens the victim line with extra charge that must be removed from the victim line when the victim line switches even though some of that charge is not used to prevent "glitching."

Thus, the need has arisen for an improved way of reducing "glitch" due to capacitive coupling between signal lines on an integrated circuit. The improved "glitch" reduction scheme should not require increased line spacing so that the overall density of the integrated circuit (and hence, the cost) is not significantly impacted. Furthermore, such an improved scheme should minimize the amount of capacitance added to the victim line so that the victim line may still switch a rapidly as possible thus maximizing the speed of the circuit.

SUMMARY OF THE INVENTION

This and other needs are met by the present invention that actively transfers charge onto the victim line as the culprit line is switching. It uses an inverter and a capacitor to dump charge onto the victim line. The input to the inverter is connected to the culprit line to sense when the culprit line is switching. In one embodiment, the capacitor is constructed from the gate of a FET.

In another embodiment, a first inverter is constructed to respond very rapidly to a falling edge on the culprit line. The output of this first inverter is connected to the drain and source of a n-channel FET. The gate of the n-channel FET is connected to the victim line. A second inverter is constructed to respond very rapidly to a rising edge on the culprit line. The output of this second inverter is connected to the drain and source of a p-channel FET. The gate of the p-channel FET is connected to the victim line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic illustration showing a charge compensation circuit and the parasitic capacitance between the culprit and the victim line.

FIG. 2 is a schematic illustration of a charge compensation circuit that uses an NFET as a capacitor to optimize charge compensation of falling edges on the culprit line and a PFET as a capacitor to optimize charge compensation of rising edges on the culprit line.

DETAILED DESCRIPTION

FIG.1 shows the charge compensation circuit and the parasitic capacitance between the culprit line **102** and the victim line **110**. The parasitic capacitance between the culprit and the victim is shown as capacitor C2 **116**. The charge compensation circuit is shown inside box **120**. P-channel field effect transistor (a.k.a. PFET) M1 **104** and n-channel field effect transistor (a.k.a. NFET) M2 **106** form a CMOS inverter that has the culprit line **102** as an input. The source of M1 is connected to the positive supply rail VDD. The gate of M1 is connected to the culprit line **102**. The drain of M1 is connected to intermediate node **112**. The source of M2 is connected to the negative supply rail GND. The gate of M2 is connected to the culprit line **102**. The drain of M2 is connected to intermediate node **112**. Capacitor C1 **108** is connected between intermediate node **112** and the victim line **110**.

To illustrate the operation of the circuit, assume that both the culprit and the victim line are discharged to a voltage at or near GND. Now assume that the culprit line starts to transition from this low state to a high state. As

the voltage on the victim line rises, current will flow from the culprit line through parasitic capacitance C2 to the victim line. This current causes the victim line to begin to accumulate charge, causing the voltage on the victim line to rise. However, as the culprit line rises, it also causes transistor M1 to turn off, and M2 to turn on. This causes intermediate node **112** to transition from a high state to a low state. As intermediate node **112** transitions, current will flow from the victim line, through capacitor C1, through transistor M2, to GND. This current serves to remove some, if not all of the charge that flowed onto the victim line through parasitic capacitance C2. The exact amount of charge that is removed from the victim line depends on the size of C1. Because the exact amount of charge that is placed on the victim line depends on C2, the size picked for C1 depends on C2, the location of the signal drivers for the culprit and victim lines, and the location of the charge compensation circuit. A typical range of sizes for C1 may be between 10% to 50% of C2. In one embodiment, C1 is chosen to be about 20% of C2 and the charge compensation circuit is located near the receiver connected to the victim line. The size picked for C1 may also be optimized by using an analog circuit simulator. The best known analog circuit simulator is SPICE, which was developed by the University of California at Berkeley and is available commercially from several companies.

FIG. 2 shows a charge compensation circuit that uses a NFET as a capacitor to optimize charge compensation of falling edges on the culprit line and a PFET as a capacitor to optimize charge compensation of rising edges on the culprit line. The culprit line **202** is connected to a first CMOS inverter comprised of PFET MP1, **204**, and NFET MN1, **206**. The output of this first inverter is connected to intermediate node A, **230**. PFET MP1 is much wider than NFET MN1 so that the output node of this first inverter, A, will switch very rapidly from a low to a high level when culprit line **202** starts changing from a high level to a low level. For example, the width of MP1 might be four times the width of MN1. Intermediate node A is connected to the source and drain of an NFET, MC1, **222**, that is being used as a capacitor. The gate of MC1 is connected to victim line **212**. Before a falling edge on the culprit can occur, the culprit line must be at a high level. Therefore, intermediate node A must be at a low level. The most important situation is to prevent a low going "glitch" on a victim line which is already at a high level. Choosing MC1 to be an NFET and connecting the gate of MC1 to the victim line maximizes the capacitance of MC1 because MC1 will have formed a channel because the gate of MC1 will be at a high level and the source and drain will be at a low level. (i.e. MC1 will be "on".) Furthermore, the parasitic capacitances associated with the drain and source diodes of MC1 are only presented to the intermediate node A and do not burden the victim line.

The culprit line **202** is also connected to a second CMOS inverter comprised of PFET MP2, **208**, and NFET MN2, **210**. The output of this second inverter is connected to intermediate node B, **232**. NFET MN2 is much wider than PFET MP2 so that the output node of this second inverter, B, will switch very rapidly from a high to a low level when culprit line **202** starts changing from a low level to a high level. For example, the width of MN2 might be three times the width of MP2. Intermediate node B is connected to the source and drain of an PFET, MC2, **220**, that is being used as a capacitor. The gate of MC2 is connected to victim line **212**. MC2 is chosen to be a PFET for similar reasons given above for choosing MC1 to be an NFET. One embodiment has each charge dump capacitor MC1 and MC2 being approximately 5% to 25% of the interline capacitance between the culprit and the victim. As before, the actual sizes of MC1 and MC2 may be optimized using an analog circuit simulator.

When the victim line switches, it will couple charge onto the culprit. Hence the roles as victim/culprit line can be reversed. Accordingly, one embodiment duplicates the circuits of FIGs. 1 and 2 and connects the additional circuits to prevent coupling from the victim lines, **110** and **212**, to the culprit lines **102** and **202**.

It is to be understood that the claimed invention is not to be limited by the preferred embodiments but encompasses other modifications and alterations within the scope and spirit of the inventive concept. For example, the invention has been described in terms of compensating for coupling charge between static signals. However, it could easily be used on signal lines carrying dynamic or pre-charge pull-down signals. The described embodiments are to be considered as illustrative and not restrictive, the scope of the invention being indicated by the claims rather than by the foregoing description.

Claims

1. A charge compensation apparatus, comprising:

   a culprit line (102) and a victim line (110), wherein there is a parasitic capacitance (116) between the culprit line (102) and the victim line (110);

   transition detecting means (104, 106) for determining when the culprit line transitions from a first voltage level to a second voltage level, the culprit line transition being accomplished by adding a first charge with a first polarity to the culprit line; and

   charge dumping means (108), responsive to the transition detecting means (104, 106), for dumping a second charge onto the victim line, said second charge having a second polarity that is the opposite polarity of the first polarity.

2. The apparatus of claim 1, wherein the charge dumping means (108) is a capacitor.

3. The apparatus of claim 2, wherein the transition detecting (104, 106) means is a CMOS inverter.

4. A charge compensation apparatus, comprising:

a culprit line (102) and a victim line (110), wherein there is a parasitic capacitance (116) between the culprit line and the victim line;
transition detecting means (104, 106) for determining when the culprit line transitions from a first voltage level to a second voltage level, the culprit line transition being accomplished by adding a first charge with a first polarity to the culprit line;
a charge dumping means (108) having a first terminal and a second terminal, the first terminal being connected to the victim line (110); and
switching means (104, 106), responsive to the transition detecting means (104, 106), for connecting the second terminal to a power supply that is approximately the first voltage level.

5. The apparatus of claim 4, wherein the charge dumping (108) means is a capacitor.

6. The apparatus of claim 5, wherein the transition detecting means (104, 106) and the switching means (104, 106) are comprised of field effect transistors.

7. A charge compensation apparatus, comprising:

a culprit line (102) and a victim line (110), wherein there is a parasitic capacitance (116) between the culprit line (102) and the victim line (110), said parasitic capacitance (116) having the effect of causing charge coupling between the culprit line (102) and the victim line (110) when the culprit line transitions between a first voltage level and a second voltage level; and
an inverter (104, 106) having an input and an output (112), the input being coupled to the culprit line (102) and the output (112) being connected to a first terminal of a charge dumping capacitor (108), wherein a second terminal of the charge dumping capacitor is connected to the victim line (110), and whereby the inverter (104, 106) switches the output (112) in response to the transition of the culprit line from the first voltage level to the second voltage level thereby reducing the effect of charge coupling between the culprit line (102) and the victim line (110) by dumping a charge on the charge dumping capacitor (108) onto the victim line (110).

8. A charge compensation apparatus, comprising:

a culprit line (202) and a victim line (212), wherein there is a parasitic capacitance between the culprit line (202) and the victim line (212);
a first charge dumping capacitor (222), said first charge dumping capacitor (222) being constructed from a n-channel field effect transistor (NFET), the NFET having a first drain and a first source and a first gate, and wherein the first gate is connected to the victim line (212);
a first inverter (204, 206), having a first input and a first output (230), the first input being coupled to the culprit line, the first output (230) being connected to the first drain and the first source;
a second charge dumping capacitor (220), said second charge dumping capacitor (220) being constructed from a p-channel field effect transistor (PFET), the PFET having a second drain and a second source and a second gate, and wherein the second gate is connected to the victim line (212); and
a second inverter (208, 210), having a second input and a second output (232), the second input being coupled to the culprit line (202), the second output (232) being connected to the second drain and the second source.

9. The apparatus of claim 8 wherein the parasitic capacitance has the effect of causing charge coupling of a first polarity between the culprit line (202) and the victim line (212) when the culprit line transitions between a first voltage level and a second voltage level, and wherein the parasitic capacitance has the effect of causing charge coupling of a second polarity between the culprit line (202) and the victim line (212) when the culprit line transitions between the second voltage level and the first voltage level, the first voltage level being higher than the second voltage level, and wherein the first inverter (204, 206) switches the first output (230) faster in response to the culprit line transitions between the first voltage level and the second voltage level than the first inverter (204, 206) switches the first output (230) in response to the culprit line transition between the second voltage level and the first voltage level.

10. The apparatus of claim 9 wherein the second inverter (208, 210) switches the second output (232) faster in response to the culprit line transitions between the second voltage level and the first voltage level than the second inverter (208, 210)

switches the second output (232) in response to the culprit line transitions between the first voltage level and the second voltage level.

11. The apparatus of claim 10 wherein the first inverter (204, 206) switches the first output (230) faster in response to the culprit line transitions between the first voltage level and the second voltage level than the second inverter (208, 210) switches the second output (232) in response to the culprit line transition between the first voltage level and the second voltage level.

FIG. 1

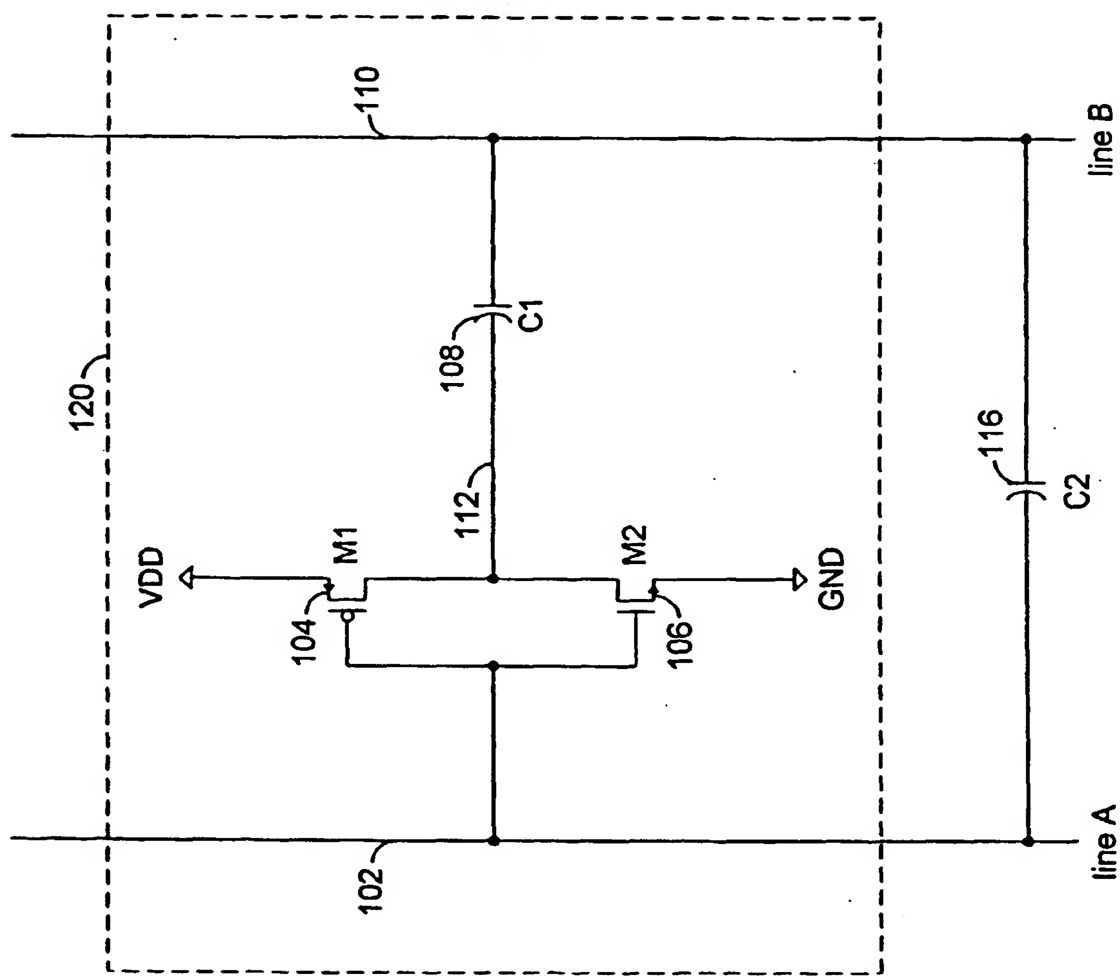
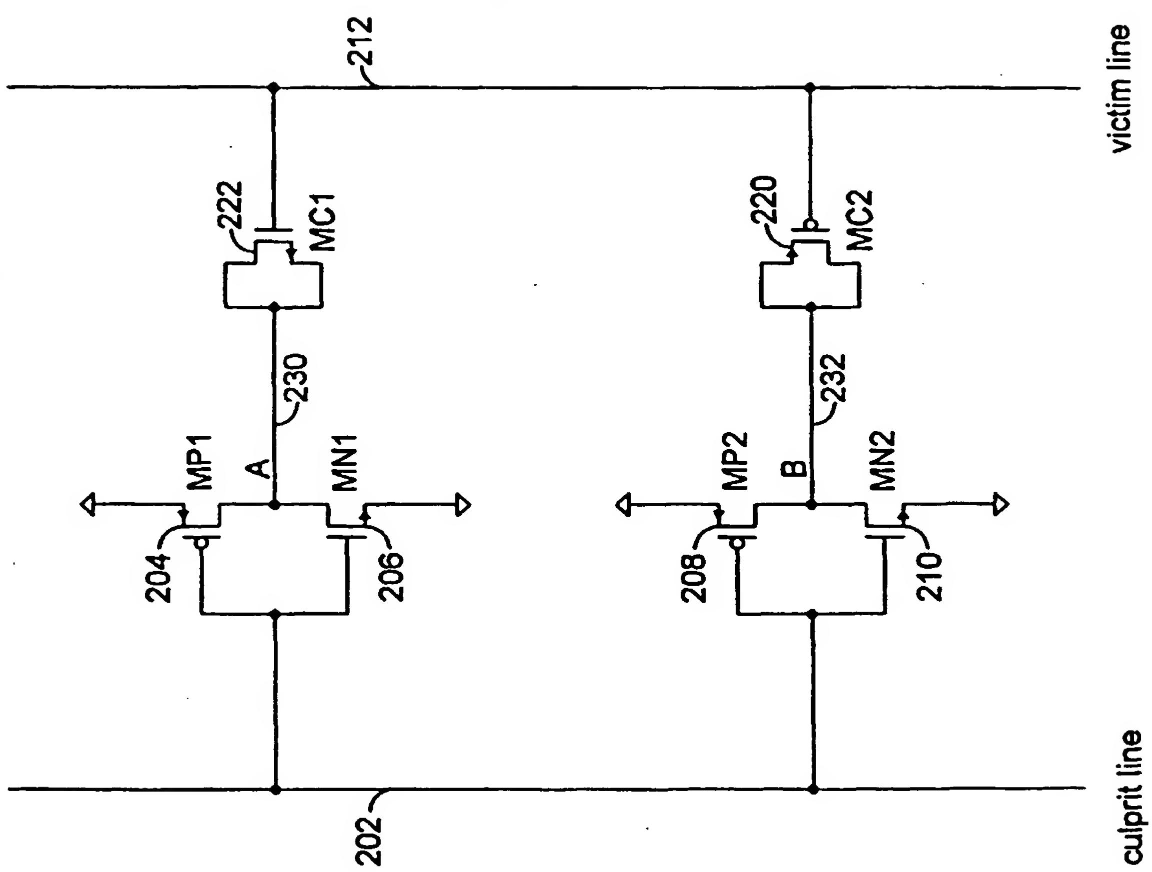


FIG. 2


212
victim line
222
MC1
220
MC2
230
232
MP1
A
MN1
MP2
B
MN2
204
206
208
210
202
culprit line

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 10 4191

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 091 661 A (CHIANG DAVID) 25 February 1992 * column 2, line 55 - column 2, line 62; claim 1; figure 6 * ---	1-8	H03K19/003
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 268 (E-0939), 11 June 1990 & JP 02 084817 A (NEC CORP), 26 March 1990, * abstract; figure 2 * -----	1-8	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	6 July 1998	Brown, J

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)